User's Guide micro-line® SC1394-1995 High Performance Serial Bus Communication Board

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1. General

1.1 Introduction

Fast, low-cost, and easy-to-handle communication systems are an important basis to connect home-PCs and various high-end multimedia devices. In order to successfully serve and satisfy consumer demands, a think-tank of engineers from many leading chip manufacturers, e. g. Texas Instruments or Intel, developed a new communication standard called IEEE 1394-1995.

ORSYS offers a fast serial high-performance bus which provides data-transmission rates of up to 200Mbit/s. In theory, 1023 buses with 63 nodes per bus can be connected. Each node has an address space of 256 tera bytes which can be accessed by any node.

The transmission medium IEEE 1394-1995 consists of two shielded, twisted-pair copper cables which are two power wires. They can carry currents of 1.5A with voltages between 8V and 40V. The standard cable length is limited to 4.5m between two nodes, although it has already been tested for much longer distances (up to 20m). In order to increase the distance, line drivers can be inserted into the cable.

The plug's contacts are closed before the IEEE 1394-1995 data lines become contact which enables the hot-plugging of all nodes of the IEEE 1394 network. After adding or removing any node, the net re-configures itself automatically by the arbiter unit on each node. The topology must not build a ring. Only tree structures are allowed.

The bus has two types of data transmission with variable data-block length:

- asynchronous data transmission (control functions)
- isochronous data transmission (huge amount of data with fixed timing)

Asynchronous data is sent to an explicit address and an acknowledgement is expected.

Isochronous data packets are sent to every participating node of the bus in constant intervals with a length of 125µs. Prior to this, a common channel number is established between the source and the target node. Isochronous data transmission needs no acknowledgement.

The communication system is divided in 3 hierarchic layers:

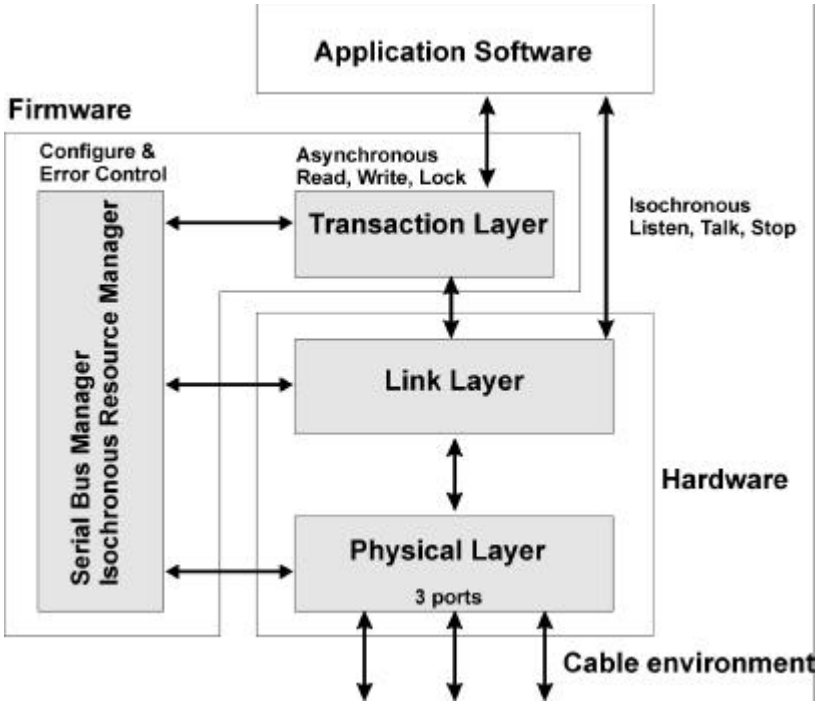
- *Transaction Layer* (3rd layer)
- *Link Layer* (2nd layer)
- *Physical Layer* (1st layer)

The hardware, consisting of the TSB21LV03 (*Physical Layer*) and the TSB12LV31 (*Link Layer*), takes over the functions of the 1st and 2nd layer. The 3rd layer (*Transaction Layer*) has to be added by software. The *Transaction Layer* reads and writes asynchronous data. The *Isochronous Resource Manger* which covers all layers, controls the isochronous data transfer. It administers channels and the bandwidth for the data transfer and controls the transfer intervals.

Higher control functions are managed by the *Bus Manger* which optimizes the capability of data transfer and manages the power supply. The layer model is shown below.

A typical application of the IEEE 1394-1995 is to connect consumer electronics devices as TVs, camcorders, stereos, mixing-desks, video-recorders, video-printers, PC video-boards, mass-memory and ATM-network-boards (for long-distance transfer) with only one cable for each device. Digital video and audio transfers are in real-time and without any quality loss.

1.2 The Basic IEEE 1394-1995 Standard



The IEEE 1394-1995 Standard for the High-Performance Serial Bus is available from the *Institut of Electrical and Electronics Engineers* for a fee of $90.00 (Order-No. *SH94364-NYF*). This standard defines all important features of this data bus, e. g. plug-in connectors, cables, signal paths, interfaces, protocols, controlling procdures, registers and many others. We recommend the IEEE 1394-1995 Standard as an additional documentation to this user's guide.

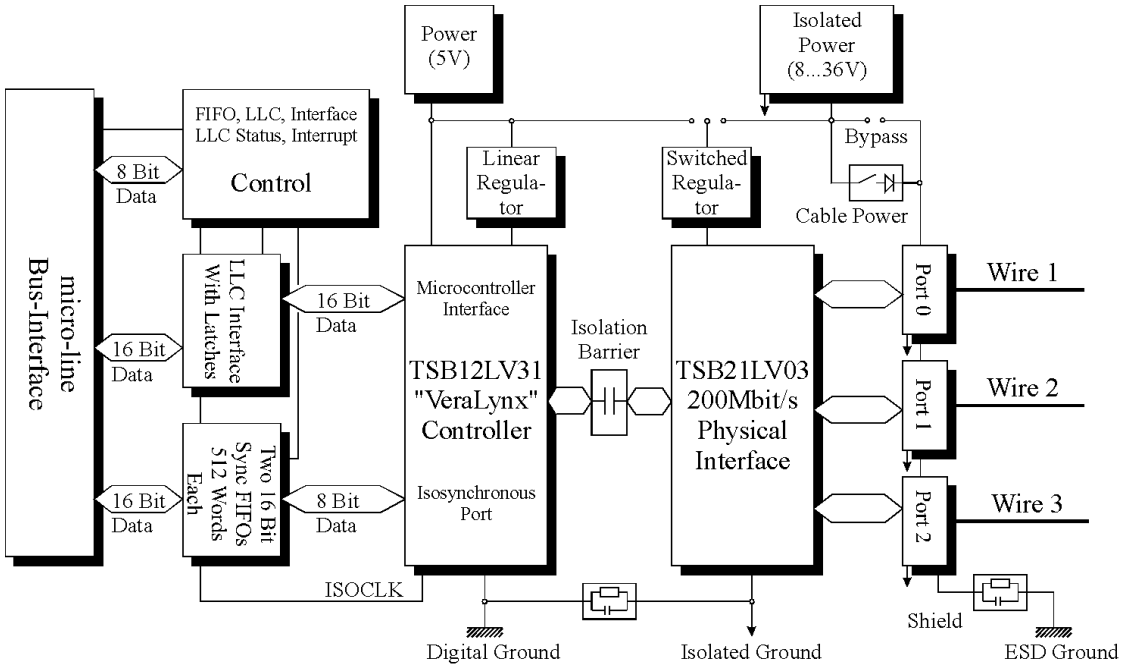
Contacts:

The Institute of Electrical and
Electronics Engineers, Inc.
345 East 47th Street
New York, NY 10017-2394
USA

Standard Ordering Service
IEEE Customer Service
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA
E-mail:
customer.service@ieee.org

2. Hardware

2.1 Block Diagram of the IEEE 1394 Serial Communication Board



2.2 The Microcontroller Interface of the LLC TSB12LV31 (Asynchronous Transfer)

Almost all data transfers between the LLC and the Controlling Processor are done via the address- and data latches of the **M**icrocontroller **I**nterface. These latches give access to the registers of the LLC and the internal asynchronous FIFO. The data exchange can be controlled by polling the two lower bits of the *Modul Status Register* (see *Interrupt Enable Register*).

Additionally, access to the LCC registers can be controlled by the READY signal. In this case, the controlling processor will be stopped until the access has been acknowledged by the LLC. This procedure may slow down the processor, but enables the fastest data exchange possible between the processor and the LLC.

The following is a description of the LLC register access in the polling mode via the MC interface:

Write access:

First there has to be a write access for the requested LLC register. After the write access, the LSB of the *Modul Status Register* has to be checked if the write access was successful. If the write access was not successful, the write to the requested LLC register has to be repeated and checked again.

Read access:

By accessing the *Modul Status Register* can be determined if there is still any ongoing data transfer between the latches and the LLC. As soon as there is no data pending on the interface, a dummy read will address the first data. At this point, the data contents are undefined. The *Modul Status Register* recognizes the completion of the data transfer initialized by the read access. Now, the next data is addressed. The contents read here is the data which was addressed by the preceding read access.

2.3 Isochronous Interface of the LLC

The Isochronous Interface is designed for a huge amount of data and is therefore equipped with FIFOs from 256K words up to 4096K words in both directions (standard 512K words). The width of the Isochronous Interface on the side of the processor is 16 bits. Read- and write accesses to the Isochronous Interface take place via the *External FIFO Access Register*. Data transfers via the Isochronous Interface are executed by either polling, interrupt or DMA. The *Interrupt Flag Register* is designed for polling and interrupt-controlled data transfers and provides information about the filling status of both FIFOs.

When writing data into the FIFO, the data will not immediately be sent to the LLC. The next steps of the data transfer are determined by the *ISOTX_RST Register* after the programmable filling status is reached. The possible transfer modes are either a single- or an automatically started transfer of one isochronous packet after the programmed filling status is reached.

2.4 The Power Supply of the IEEE 1394 Serial Communication Board

The board is supplied with a voltage of 5V. The voltage of 3.3V necessary for the LLC TSB12LV31 is generated from the 5V-supply in a linear way. The standard demands a galvanically isolated voltage between 8V and 40V to generate the 3.3V supply of the Phy Transceiver TSB21LV03 and to supply the current to the connected cables. This isolated voltage is connected **additionally** to the module by either the micro-line® connector P (see page 17) or by the EPS (external power supply) plug. In order to switch the galvanically isolated voltage on the cable, a programmable switch was designed.

The Phy Transceiver TSB21LV03 can also be supplied by the connected cable. In this case, additional galvanically isolated voltage is not necessary.

2.5 The Display Function of the LEDs

The IEEE 1394 Serial Communication Board SC1394-1995 has one red and two green LEDs.

The red LED is programmable via register and can be used for various display functions.

The two green LEDs D4 (besides the red LED) and D3 (the LED on the outside) are connected to the programmable status bits *STAT0* and *STAT1* of the LLC and display the specific LLC status of the FIFO. During standard setting, the LED D4 shows that the internal LLC-Receive-FIFO is full (*STAT0=1*). The LED D3 light is on when the internal LLC-Send-FIFO is empty (*STAT1=1*). The programming of the status bits *STAT0* und *STAT1* is described in the data sheet of the TSB12LV31.

3. Description of Registers

This paragraph describes the registers on the IEEE 1394 Serial Communication Board. Direct access to the registers of the IEEE1394 Serial Communication Board is usually not necessary as most of the board's functions already have C-driver object codes. The paragraph 'Software' describes the driver functions.

3.1 Address Space (Register Addresses)

The Address Space of the board consists of the Configuration Register Block of the LLC (Link Layer Controller) which allows access to the physical cable transceiver/arbiter.

The FIFO Access Register and several FIFO and ISO Control Registers are for data transfer via the Isochronous Interface of the LLC. The registers are for controlling-interrupt handling, polling or other common functions of the board.

The board's basic address is determined by one of the chip-selected input signals /CS1 to /CS7 of the micro-line® bus. The connected processor board generates the /CSx signal which can be chosen by putting the corresponding solder bridge on the IEEE1394 Serial Communication Board. The address pins A0 to A8 can additionally be used for further decoding of the individual registers on the IEEE1394 Serial Communication Board.

Therefore, the Address Space of the board includes the addresses *Base+00h* to *Base+1FFh*.

3.1.1 The Configuration Registers of the LLC (Link Layer Controller) (00h-50h)

Offset-Address	Register Name
00h	Version Register
04h	MISC Register
08h	Control Register
0Ch	Interrupt Register
10h	Interrupt Mask Register
14h	Cycle Timer Register
18h	IsoPort Number Register
1Ch	reserved
20h	Diagnostic Register
24h	Phy Access Register
28h-2Fh	reserved
30h	ATF Status Register
34h	Bus Reset Register
38h	Self-ID Check Register
3Ch	GRF Status Register
40h-4Fh	reserved
50h	FIFO State Register

3.1.2 LLC Register for Isochronous Data Transmission (54h-7Fh)

Offset-Address	Register Name
54h	Isochronous Control Register
58h	Isochronous Mode Register
5Ch	Isochronous Header Register
60h-7Fh	reserved

3.1.3 LLC Register for Internal FIFO Access (80h-FFh)

Offset-Address	Register Name
80h	ATF_First
84h	ATF_Continue
88h	reserved
8Ch	ATF_Continue & Update
90h-BFh	reserved
C0h	GRF Data
C4h-FFh	reserved

3.1.4 Register for FIFO Transfer, Interrupt and other Functions (100h-1FFh)

Offset-Address	Register Name
100h	Module Status / Module Control Register
101h	Interrupt Enable / Interrupt Flag Register
102h	External TXFIFO Program Register
103h	ISO Status Register / ISOTX_RST
104h-17Fh	reserved
180h-1FFh	External FIFO Access Register

3.2 Register Description of the Board

The registers of the LLC are described in detail in the data sheet of the LLC *(TSB12LV31 Data Manual, Lit.Nr. SLIS255).* The corresponding offset addresses are shown in chapters *3.1.1*, *3.1.2* and *3.1.3*. Therefore, the following chapters describe only the registers which are not included in the LLC (see capture 3.1.4).

3.2.1 Module Status Register MSR and Module Control Register MCR

The Module Status Register and the Module Control Register have the same address. The Module Status Register is a read only and the Module Control Register is a write only register.

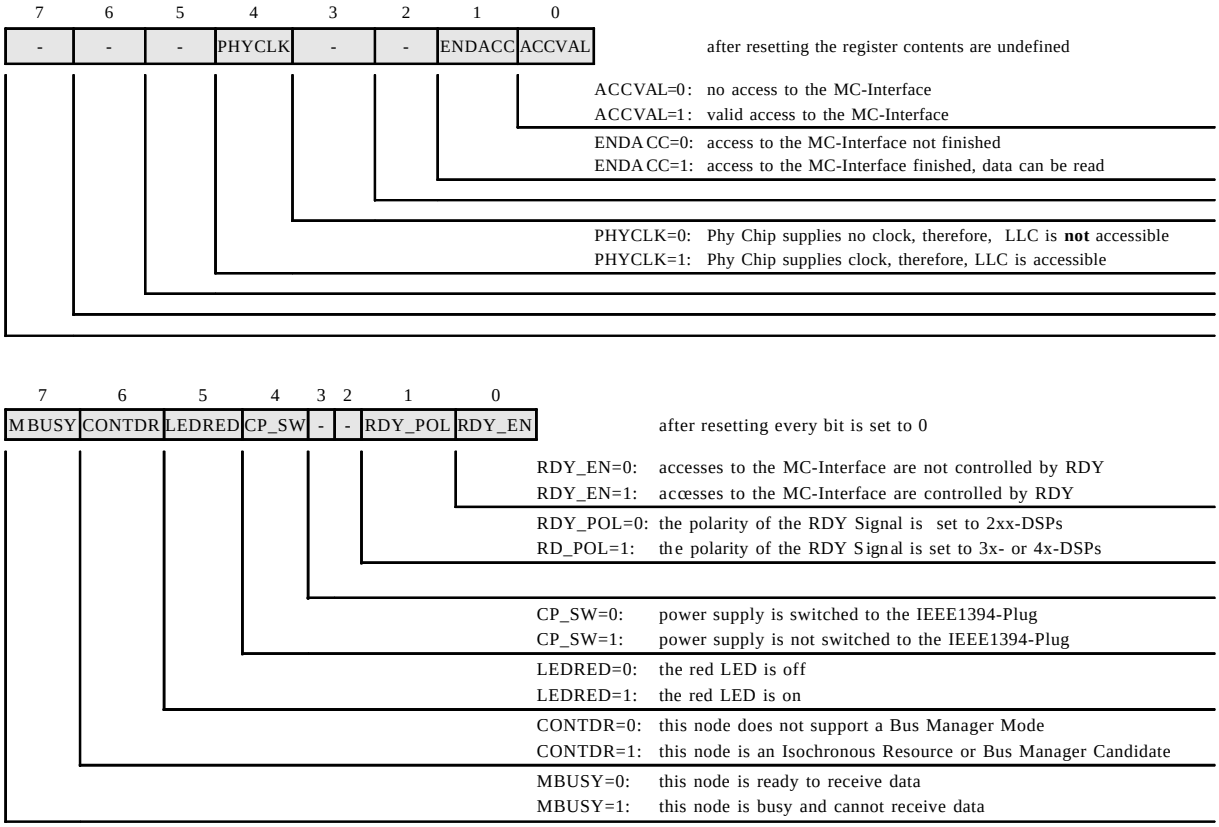
The Module Status Register contains status bits for accessing the microcontroller interface of the LLC and status bits for receiving data from the IEEE 1394 interface. After reset, the contents of the Module Status Register are undefined.

The Module Control Register controls the access to the microcontroller interface, switches the power supply to the IEEE 1394 plugs, controls the red LED, and switches the Bus Manager Mode or the Busy Mode on and off.

After a reset, the contents of the control register are set to zero.

The functions of the bits and their position within both registers are shown below.

Module Status Register (Offset 100h, read only):


7 6 5 4 3 2 1 0
- - - PHYCLK - - ENDACC ACCVAL
after resetting the register contents are undefined
ACCVAL=0: no access to the MC-Interface
ACCVAL=1: valid access to the MC-Interface
ENDACC=0: access to the MC-Interface not finished
ENDACC=1: access to the MC-Interface finished, data can be read
PHYCLK=0: Phy Chip supplies no clock, therefore, LLC is not accessible
PHYCLK=1: Phy Chip supplies clock, therefore, LLC is accessible
7 6 5 4 3 2 1 0
MBUSY CONTDR LEDRED CP_SW - - RDY_POL RDY_EN
after resetting every bit is set to 0
RDY_EN=0: accesses to the MC-Interface are not controlled by RDY
RDY_EN=1: accesses to the MC-Interface are controlled by RDY
RDY_POL=0: the polarity of the RDY Signal is set to 2xx-DSPs
RD_POL=1: the polarity of the RDY Signal is set to 3x- or 4x-DSPs
CP_SW=0: power supply is switched to the IEEE1394-Plug
CP_SW=1: power supply is not switched to the IEEE1394-Plug
LEDRED=0: the red LED is off
LEDRED=1: the red LED is on
CONTDR=0: this node does not support a Bus Manager Mode
CONTDR=1: this node is an Isochronous Resource or Bus Manager Candidate
MBUSY=0: this node is ready to receive data
MBUSY=1: this node is busy and cannot receive data

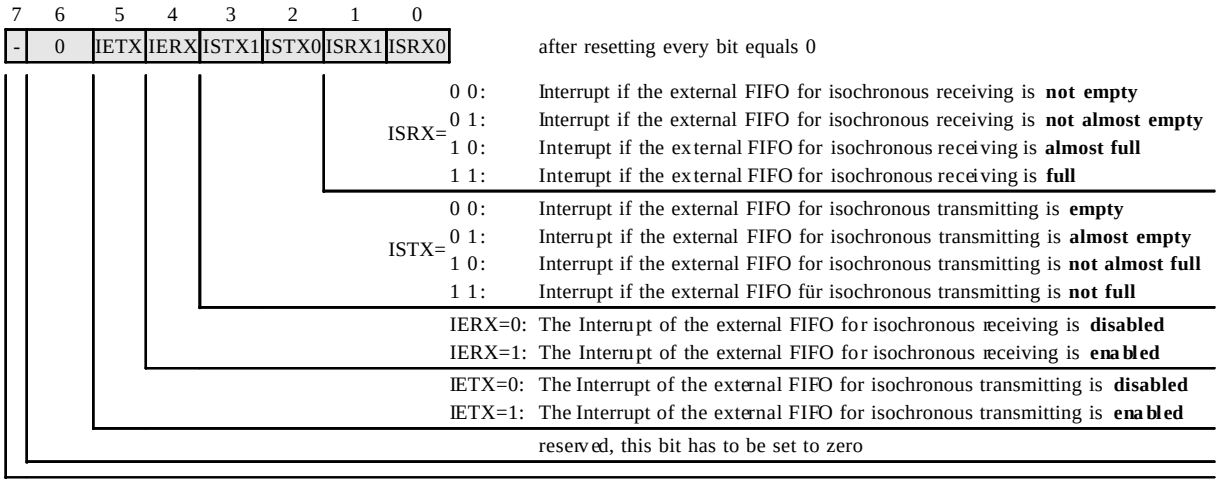
3.2.2 The Interrupt Enable and Interrupt Flag Register

The Interrupt Enable Register and the Interrupt Flag Register have the same address. The Interrupt Enable Register is write only and the Interrupt Flag Register is read only.

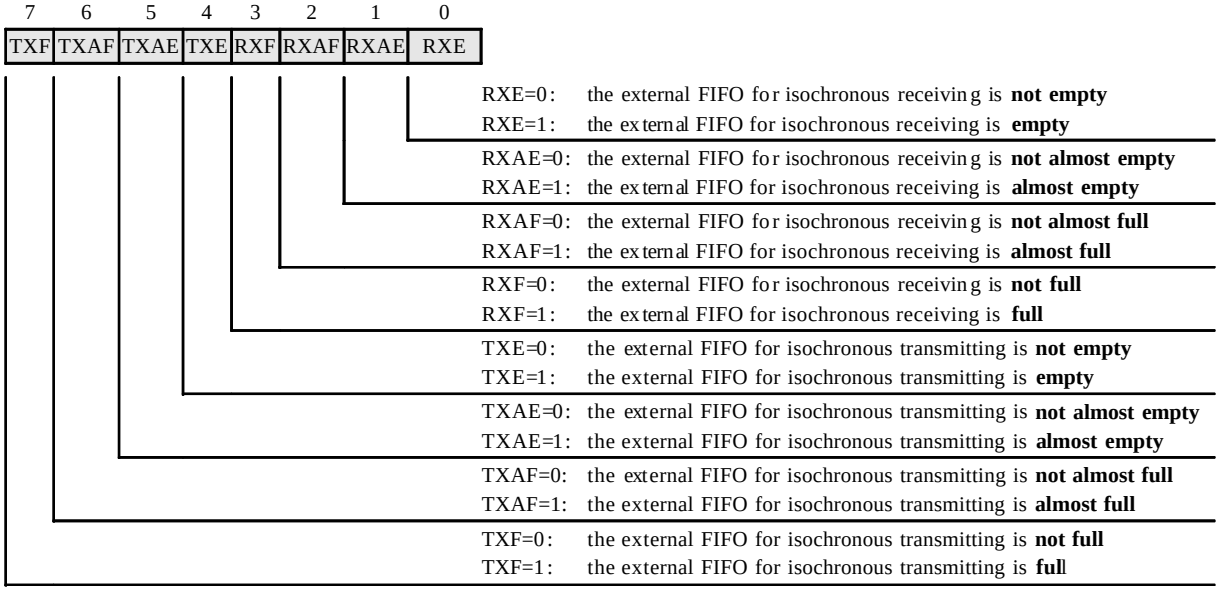
The Interrupt Enable Register selects the filling status *empty, almost empty, almost full and full* of the external FIFOs to assert an interrupt to the connected processor and sets off the two interrupt requests *FIFO receive interrupt and FIFO transmit interrupt.* After resetting the board, the Interrupt Enable Register is set to zero and consequently all interrupt requests are disabled.

The filling status of the external FIFO for transmitting and receiving can be called up by the Interrupt Flag Register. It shows the reason why the interrupt was requested. The meaning of the bits and their position in the registers are described below.

Interrupt Enable Register (Offset 101h, write only):


7 6 5 4 3 2 1 0
- 0 IETX IERX ISTX1 ISTX0 ISRX1 ISRX0
after resetting every bit equals 0
ISRX= 0 0: Interrupt if the external FIFO for isochronous receiving is not empty
0 1: Interrupt if the external FIFO for isochronous receiving is not almost empty
1 0: Interrupt if the external FIFO for isochronous receiving is almost full
1 1: Interrupt if the external FIFO for isochronous receiving is full
ISTX= 0 0: Interrupt if the external FIFO for isochronous transmitting is empty
0 1: Interrupt if the external FIFO for isochronous transmitting is almost empty
1 0: Interrupt if the external FIFO for isochronous transmitting is not almost full
1 1: Interrupt if the external FIFO für isochronous transmitting is not full
IERX=0: The Interrupt of the external FIFO for isochronous receiving is disabled
IERX=1: The Interrupt of the external FIFO for isochronous receiving is enabled
IETX=0: The Interrupt of the external FIFO for isochronous transmitting is disabled
IETX=1: The Interrupt of the external FIFO for isochronous transmitting is enabled
reserved, this bit has to be set to zero

Interrupt Flag Register (Offset 101h, read only):


7 6 5 4 3 2 1 0
TXF TXAF TXAE TXE RXF RXAF RXAE RXE
RXE=0: the external FIFO for isochronous receiving is not empty
RXE=1: the external FIFO for isochronous receiving is empty
RXAE=0: the external FIFO for isochronous receiving is not almost empty
RXAE=1: the external FIFO for isochronous receiving is almost empty
RXAF=0: the external FIFO for isochronous receiving is not almost full
RXAF=1: the external FIFO for isochronous receiving is almost full
RXF=0: the external FIFO for isochronous receiving is not full
RXF=1: the external FIFO for isochronous receiving is full
TXE=0: the external FIFO for isochronous transmitting is not empty
TXE=1: the external FIFO for isochronous transmitting is empty
TXAE=0: the external FIFO for isochronous transmitting is not almost empty
TXAE=1: the external FIFO for isochronous transmitting is almost empty
TXAF=0: the external FIFO for isochronous transmitting is not almost full
TXAF=1: the external FIFO for isochronous transmitting is almost full
TXF=0: the external FIFO for isochronous transmitting is not full
TXF=1: the external FIFO for isochronous transmitting is full

3.2.3 External TXFIFO Program Register

The external FIFOs for isochronous data transfer allow the programming of the two status bits AEF (Almost Empty Flag) and AFF (Almost Full Flag) via the corresponding FIFO-internal registers *Empty Offset* and *Full Offset*. After resetting the FIFOs, the contents of the two offset registers are always 7. This standard setting can be changed for the transmission FIFO.

The TXFIFO Program Register enables the access to the 16-bit wide registers *Empty Offset* and *Full Offset*. The write procedure to program the offset values **almost empty** and **almost full** is described below:

The TXFIFO Program Register (Offset 102h, write only) is written byte to byte.

- When first accessing the TXFIFO Program Register, the lower byte of the register *Empty Offset* is written.
- When accessing the TXFIFO Program Register for the second time, the higher byte of the register *Empty Offset* is written.
- When accessing the TXFIFO Program Register for the third time, the lower byte of the register *Full Offset* is written.

- When accessing the TXFIFO Program Register the fourth time, the higher byte of the register *Full Offset* is written.

The next access to the TXFIFO Program Register again overwrites the lower byte of the register *Empty Offset* which is corresponding to the first access.

The Offset Registers, however, cannot be read.

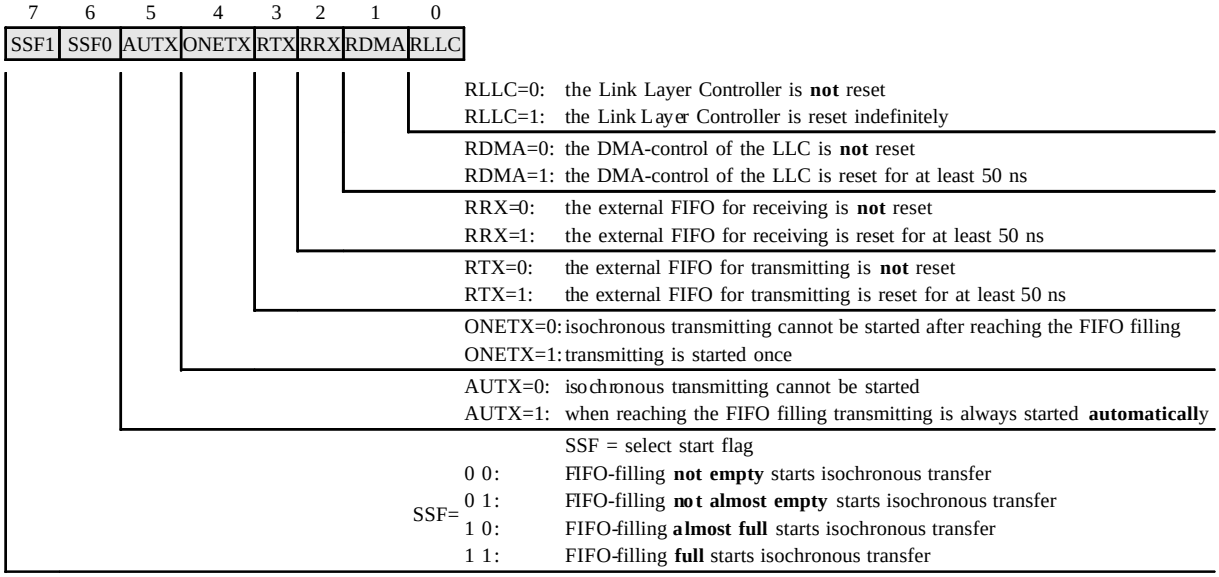
3.2.4 ISOTX_RST Register

The ISOTX_RST Register has three different functions:

- The first function of the ISOTX_RST Register is to reset some components of the board, e. g., the LLC, the Phy Unit, the DMA control of the LLC and the external FIFOs for isochronous transfer to transmit and receive data.
- The second function of the ISOTX_RST Register is to select one of the two possible transmission modes for the isochronous transfer. One transmission mode is to start the transmission of a data packet once, after reaching a programmed filling status. The other transmission mode is to start transmission of a data packet automatically more often, after reaching a programmed filling status.
- The third function of the ISOTX_RST Register is to program the filling status. Programmable FIFO fillings *are not empty*, *not almost empty*, *almost full* and *full*.

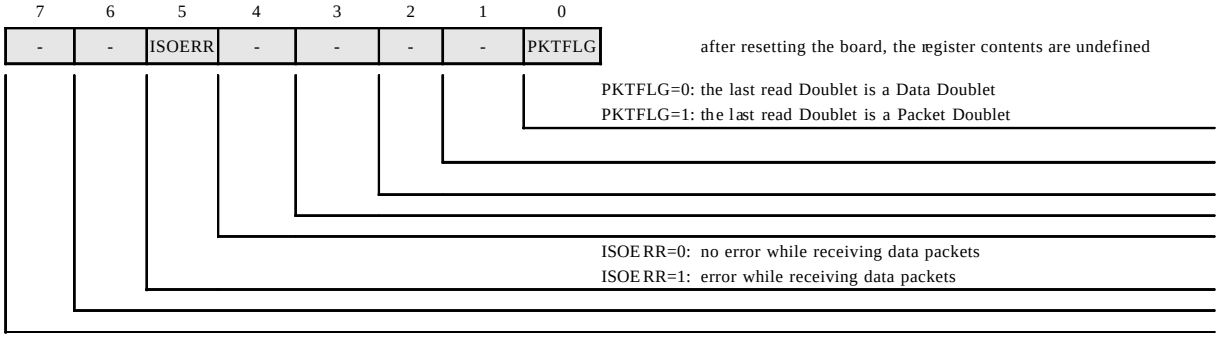
The meaning of the bits and their position in the ISOTX_RST Register is described below.

ISOTX_RST Register (Offset 103h, write only):


7 6 5 4 3 2 1 0
SSF1 SSF0 AUTX ONETX RTX RRX RDMA RLLC
RLLC=0: the Link Layer Controller is **not** reset
RLLC=1: the Link Layer Controller is reset indefinitely
RDMA=0: the DMA-control of the LLC is **not** reset
RDMA=1: the DMA-control of the LLC is reset for at least 50 ns
RRX=0: the external FIFO for receiving is **not** reset
RRX=1: the external FIFO for receiving is reset for at least 50 ns
RTX=0: the external FIFO for transmitting is **not** reset
RTX=1: the external FIFO for transmitting is reset for at least 50 ns
ONETX=0: isochronous transmitting cannot be started after reaching the FIFO filling
ONETX=1: transmitting is started once
AUTX=0: isochronous transmitting cannot be started
AUTX=1: when reaching the FIFO filling transmitting is always started **automatically**
SSF = select start flag
SSF= 0 0: FIFO-filling **not empty** starts isochronous transfer
0 1: FIFO-filling **not almost empty** starts isochronous transfer
1 0: FIFO-filling **almost full** starts isochronous transfer
1 1: FIFO-filling **full** starts isochronous transfer

After resetting, the LLC must not be accessed for a period of at least 60 us because no valid accesses to the LLC are generated during this period of time.

3.2.5 ISO Status Register


7 6 5 4 3 2 1 0
- - ISOERR - - - - PKTFLG
after resetting the board, the register contents are undefined
PKTFLG=0: the last read Doublet is a Data Doublet
PKTFLG=1: the last read Doublet is a Packet Doublet
ISOERR=0: no error while receiving data packets
ISOERR=1: error while receiving data packets

The ISO Status Register recognizes transmission errors during isochronous data transfer and differentiates Data Quadlets from the Packet Quadlets *Header and Trailer.* Accesses to the ISO Status Register should always be made after accesses to the External FIFO Register. The two Bits ISOERR and PKTFLG can be requested by the Status Register. A transmission error has occurred during the last data transfer if the ISOERR Bit is set to one. The last read contents of the External FIFO Access Register are not a Data Doublet but a Packet Doublet if the PKTFLG bit is set to one.

Please note that two Doublets which are consecutively read from the External FIFO Access Register form a Quadlet.

3.2.6 External FIFO Access Register

The exchange of isochronous data between the processor and the IEEE 1394 Serial Communication Module takes place via the external FIFO Access Register. A read access to one of the addresses *Base+100h* to *Base+1FFh* transfers 16-bit wide, isochronously-received data (Doublet-aligned) from the FIFO to the processor. A write access to one of the addresses *Base+180h* to *Base+FFh*, transfers isochronously-sent, 16-bit wide data from the processor to the FIFO.

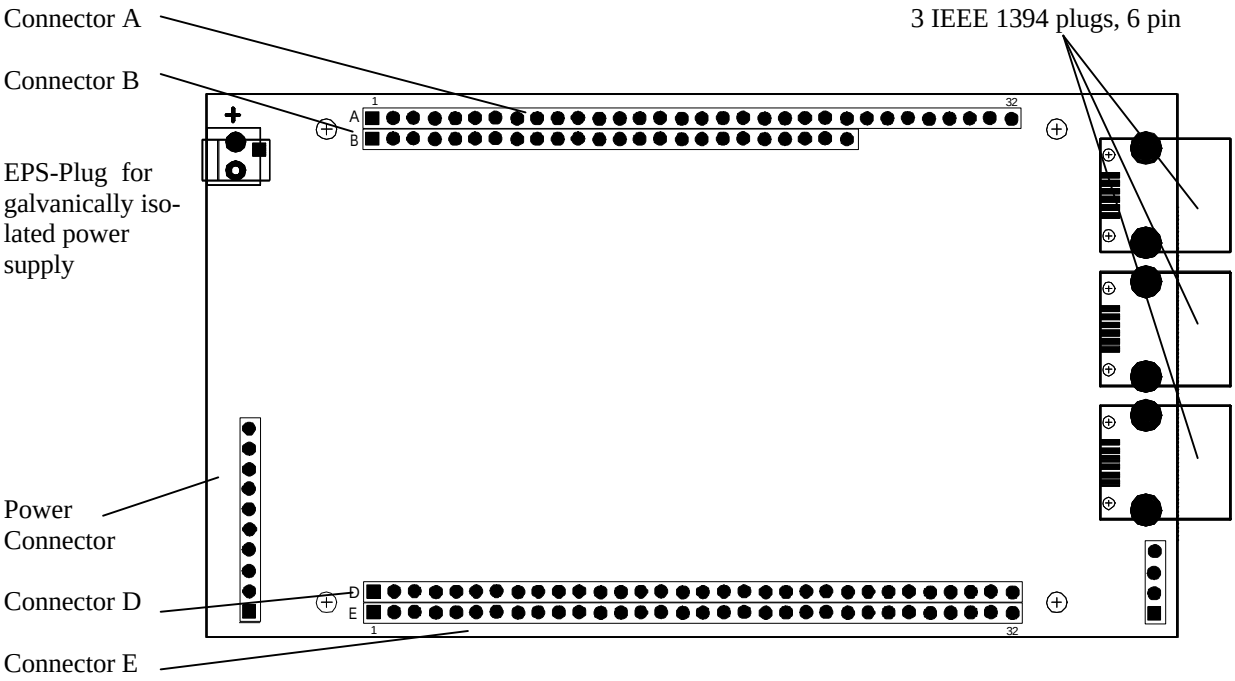
When accessing the FIFO, it is very important to determine the corresponding status bits for the filling status, unless the access is controlled by DMA or by interrupt.

The number of bytes of an isochronously-sent data block always has to be dividable by four, i.e., that only even numbers of 16-bit wide words can be written to or read from the FIFO.

4. Software

5. Connections of the IEEE 1394 Serial Communication Board

5.1 Positions of the Individual Connectors



5.2 Pin-Description and Pin-Wiring

Pin	Connector A	Connector B	Connector D	Connector E	Connector P	IEEE1394
1	D00(I/O)	A00(I)	GND (I)	-	-	VP (I/O)
2	D01(I/O)	A01(I)	GND (I)	-	-	VG (I/O)
3	D02(I/O)	A02(I)	GND (I)	-	-	TPBx- (I/O)
4	D03(I/O)	A03(I)	GND (I)	-	-	TPBx (I/O)
5	D04(I/O)	A04(I)	+5V (I)	-	-	TPAx- (I/O)
6	D05(I/O)	A05(I)	+5V (I)	-	ISO+8..30V (I)	TPAx (I/O)
7	D06(I/O)	A06(I)	-	-	ISOGND (I)	CSHLD
8	D07(I/O)	A07(I)	/RESET (I)	-	-	CSHLD
9	D08(I/O)	A08(I)	-	-	Cable Power	
10	D09(I/O)	-	/CS1 (I)	-	Cable GND	
11	D10(I/O)	-	/CS2 (I)	-		
12	D11(I/O)	-	/CS3 (I)	-		
13	D12(I/O)	-	/CS4 (I)	-		
14	D13(I/O)	-	/CS5 (I)	-		
15	D14(I/O)	-	/CS6 (I)	-		
16	D15(I/O)	-	/CS7 (I)	-		
17	-	-	/INT0 (O)	-		
18	-	-	/INT1 (O)	-		
19	-	-	/INT2 (O)	-		
20	-	-	/INT3 (O)	-		
21	-	-	-	-		
22	-	-	-	-		
23	-	-	-	-		
24	-	-	R/W (I)	-		
25	-		/STRB (I)	-		
26	-		-	-		
27	-		-	-		
28	-		-	-		
29	-		-	-		
30	-		READY (O/Z)	-		
31	-		-	-		
32	-		-	-		

5.3 Pin-Description

5.3.1 Connector A

D00...D15:

These are the bi-directional data lines of the micro-line® interface. During a reset, the lines are switched to high-impedance state.

5.3.2 Connector B

A00...A08:

These pins are the address lines of the micro-line® interface and are only inputs.

5.3.3 Connector D

GND:

The IEEE 1394 Serial Communication Board has four *Ground* power-supply pins. The potential of the pins which are not galvanically isolated is the ground for all parts of the Link Layer Controller domain.

+5V:

The IEEE 1394 Serial Communication Board has two *+5V* power-supply pins, which supply all parts of the Link Layer Controller domain. A maximum voltage of *+5.5V* is allowed.

/RESET:

All components on the board are reset, when the reset input (active low) of the IEEE 1394 Serial Communication board is activated.

/CS1.../CS7:

Chip Select Input (active low). The IEEE 1394 Serial Communication Board offers a selection of seven Chip Select Signals. One of these signals has to be selected by a solder bridge to enable write- and read accesses to the IEEE 1394 Serial Communication Board. When using several peripheral boards at the same time, each board needs its own Chip Select Signal. Therefore, the peripheral boards are decoded with different I/O addresses of the processor board.

/INT0.../INT3:

Interrupt outputs (active low, open collector) of the IEEE 1394 Serial Communication Board. The three internal interrupt signals of the IEEE 1394 Serial Communication Board */INTLLC*, */RXINT* and */TXINT* can be switched by solder bridges to any of the interrupt outputs */INT0* to */INT3*.

For example, all internal interrupt signals can be switched to one interrupt output, or several interrupt signals can be switched to different interrupt outputs.

R/W:

The read/write input signal on the micro-line® bus. A read cycle occurs if the signal is 'high' and a write cycle occurs if the signal is 'low'.

/STRB:

The Strobe Input Signal (active low) indicates a read- or write access. The address on the address bus is valid if the signal is active.

READY:

The Bus Ready Output Signal (active high, active low or tri-state) can be used to insert additional I/O wait states to external bus cycles until a read- or write access to the MC interface of the LLC is finished. While additional wait states are inserted (READY is inactive), all signals of the external memory bus (address-, data- and control signals) are held in their state until the READY Signal becomes active again. The use of the READY Signal is programmable. If the READY Signal is enabled, it changes from high-impedance state to low-impedance state. It is important that the polarity of the READY Signal is adjusted to the applicable processor type before the READY Signal is enabled (see Modul Control Register). After resetting the board and also during I/O accesses of the processor, the READY Signal is always set to high-impedance state.

5.3.4 Connector P and EPS-Plug

The power supply of the IEEE 1394 transceiver of the physical layer and the nodes which are connected to the cable require a galvanically isolated voltage between 8V and 30V. This voltage can be supplied to the board by either the connector P (power supply) or by the EPS-plug (External Power Supply). The maximum current is 1.5A.

ISO+8..30V

Power supply for the IEEE 1394 transceiver and the cable.

ISOGND:

ISOGND is the ground for the galvanically isolated voltage of the IEEE 1394 transceiver and the cable.

Cable power:

Directly connected to the VP power-supply line of the cable. This pin is used if the Link Layer and other devices are powered by cable.

Cable GND:

Cable GND is the ground for the galvanically isolated voltage of the IEEE 1394 transceiver and the cable.

5.3.5 IEEE 1394 Plug

On the board are altogether three IEEE 1394-1995 plugs type "flat, smd" installed. They are numbered 1 to 3. The corresponding names of the data connections are: *TPA1* to *TPA3*, *TPA1-* to *TPA3-*, *TPB1* to *TPB3* and *TPB1-* to *TPB3-*. In place of the index, there is an 'x' in the connection description.

VP:
According to standard, the power supply of the nodes connected with the IEEE 1394 cable is between 8V and 40V.

VG:
The ground of the galvanically isolated voltage is the same as of ISOGND.

TPBx, TPBx-:
Twisted cable pair B for data transfer via the IEEE 1394 connector.

TPAx, TPAx-:
Twisted cable pair A for data transfer via the IEEE 1394 connector.

6. Solder Bridges

There are 25 solder bridges on the IEEE 1394 Serial Communication Board. Under normal conditions, there is no need to change their position (soldered or not soldered). The solder bridges J24 and J33 determine the kind of power supply and the power-supply source. The bridges PC1 and PC2 are directly connected with the equally-named input signals of the Physical Transceivers 21LV03. Their purpose is to provide information about the board's provided or needed power. The solder bridge J26 adjusts the isolation between the LLC and the Physical Transceiver.

Further solder bridges select the Chip Select Signal*/CSx* of the board and switch the internal Interrupt Signals to the requested external Interrupt Signals /INT0 to /INT3.

6.1 Positions and Functions of the Solder Bridges

The description, positions and functions of the solder bridges on the rear of the board are explained below:

6.1.1 Solder Bridges to determine Power Supply and Galvanical Isolation

Solder bridge J24 selects the voltage for the PWM Converter which supplies the Physical Transceiver with 3.0V.

- When solder bridge J24 is in position 3-2, the PWM Converter is supplied by the cable or the EPS-Plug or the P-Connector.

- When solder bridge J24 is in position 1-2, the PWM Converter is supplied by the **not** galvanically isolated voltage (+5V) of the LLC.

The two grounds ISOGND and GND have to be connected by solder bridge J33 if the PWM Converter is supposed to be supplied by the **not** galvanically isolated voltage (+5V) of the LLC.

The galvanic isolation between the LLC and the Physical Transceiver is realized by Decoupling-Capacitors in the data-transmission lines. Solder bridge J26 must not be set if these Decoupling-Capacitors are replaced by zero-ohm-resistors.

When operating in the galvanically isolated mode, solder bridge J26 is soldered, solder bridge J24 is in position 1-2, and solder bridge J33 is not soldered.

6.1.2 Solder Bridges to determine the Power Class Information

The Power Class Information of the board is set by the solder bridges PC1 and PC2. They provide information about the power provided or needed from the board. The Physical Transceiver reads the positions of the bridges which are signaled to other nodes of the system by the *Self-ID Packet* . The relation between power class and the status of the solder bridges PC1 and PC2 is explained in the two tables below:

The first table applies to nodes providing power to the cable:

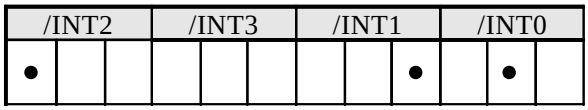
PC1	PC2	explanation
-	-	this node does not need and does not provide power
-	closed	this node is self-powered and provides a minimum of **15W** to the bus
closed	-	this node is self-powered and provides a minimum of **30W** to the bus
closed	closed	this node is self-powered and provides a minimum of **45W** to the bus

The second table applies to nodes which are powered by cable:

PC1	PC2	explanation
-	-	this node can be powered from the bus and uses up to **1W**
-	closed	this node is powered from the bus and uses up to **1W**. An additional **2W** is needed to enable the LLC and higher layers
closed	-	this node is powered from the bus and uses up to **1W**. An additional **5W** is needed to enable the LLC and higher layers
closed	closed	this node is powered from the bus and uses up to **1W**. An additional **9W** is needed to enable the LLC and higher layers

6.1.3 Solder Bridges to switch the Internal Interrupt to the Connections /INT0 to /INT3

The board uses three interrupts. The */INTLLC* signal is in accordance with the output signal */INT* of the LLC. The */RXINT* and */TXINT* signals control the transfer between the Processor and the LLC or the external FIFO for isochronously transmitted data. These three interrupts can be switched to the */INT2*, */INT3*, */INT1* and */INT0* pins by solder bridges. It is possible to connect all three internal interrupts to one */INTx pin*. It is not allowed and irrational to connect a single interrupt with more than one */INTx pin*. In general, only one interrupt is connected with one */INTx pin*. The example below shows the connection between */INTLLC* and */INT2*, */TXINT* and /*INT1* and */RXINT* and */INT0*.



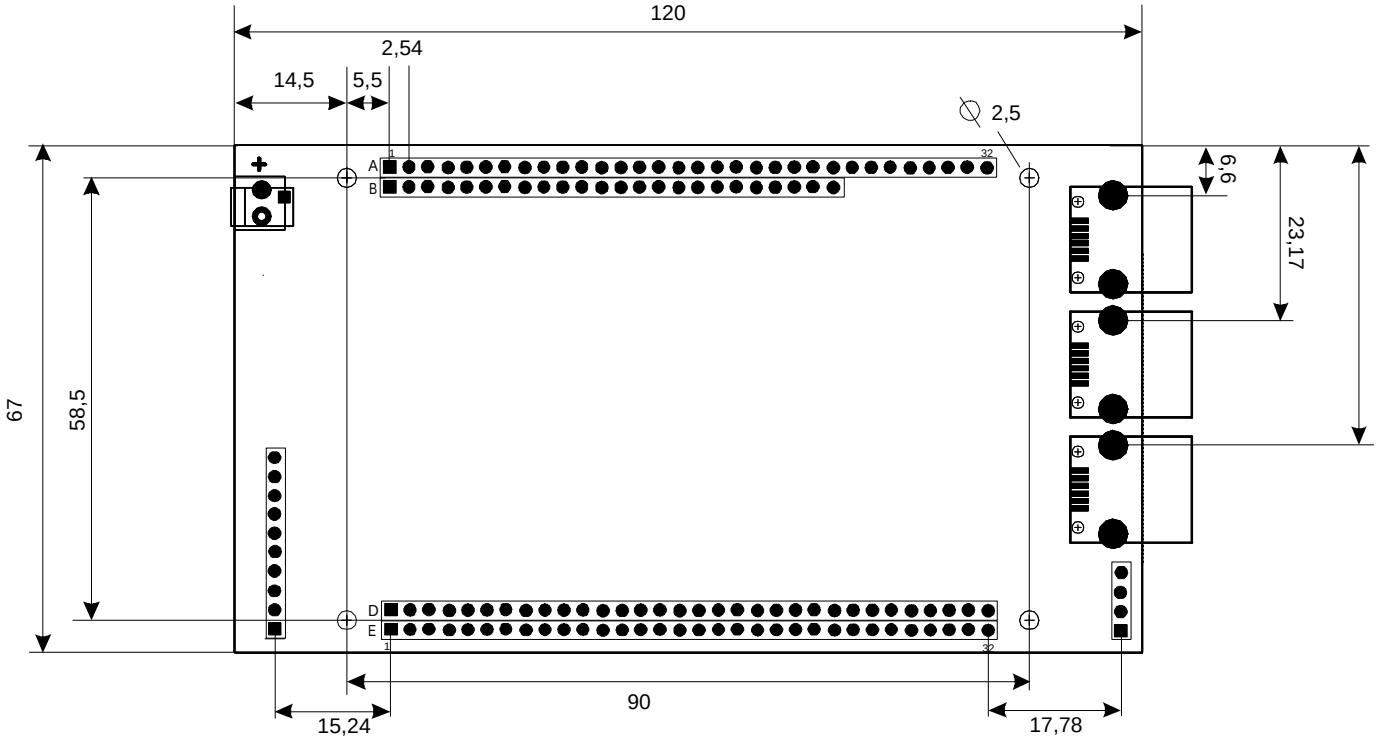
7. Other

7.1 Power Consumption

Unit	Minimum-consumption [1)]	Maximum-consumption [2)]
Phy Transceiver Area		
LLC Area		

7.2 Board Dimensions

All dimensions in mm



7.3 Ambient Temperature

Storage temperature: -25...+85^{0} C
Operating temperature: 0...70^{0} C

7.4 Ambient Humidity

Storing with up to 90% humidity, not thawing.
Operating with up to 85% humidity, not thawing.